Nayan Ramam

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Education

Georgia Institute of Technology | Atlanta, GA *August 2024 – Present*

B.S. in Electrical Engineering, GPA 3.95, Dean's List, IEEE-Eta Kappa Nu Honor Society Expected Graduation, December 2027

Relevant Coursework: Analog CMOS IC Design, Analog Electronics, Microelectronics, Signal Processing, Digital Design Lab

Skills

Programming Languages: SystemVerilog, Verilog, VHDL, Python, RISC-V, C

Software/Platforms: Cadence Virtuoso/ADE/Spectre/Pegasus, KiCAD, PyTorch, OpenCV, scikit-learn, Linux, Quartus, Git

Hardware: Field Programmable Analog Array (FPAA), FPGA, Oscilloscope, DMM, Arduino/Teensy, Raspberry Pi, Daisy Seed

Experience

ASIC Verification/Design Intern | Hewlett Packard Enterprise *May 2026 – August 2026*

- Summer intern on the Aruba Networking Post-Silicon/Emulation team

Analog Mixed-Signal Researcher | Integrated Computational Electronics Lab *October 2025 – Present*

- Building audio synthesis/signal processing circuit library on FPAA (VCO, Gilbert multiplier, envelope generator, etc.)
- Tuning and validating using Digilent Analog Discovery, Function Generator, Oscilloscope
- Developing Python to Verilog netlist to GDSII compiler to allow for analog HLS

Team Lead + Lead Researcher | Math Modeling Student Research Group *August 2024 – April 2026*

- Led mechanistic interpretability research team quantifying polysemanticity in convolutional neural networks
- Developed a Python pipeline to generate and embed feature visualizations via gradient ascent (PyTorch, NumPy)
- Formulated a novel scoring metric that incorporates cluster count, angular separation, and density metrics

Digital Design/Hardware Systems Researcher | San José State University *May 2025 – August 2025*

- Adapted Analog Devices' IP for JESD204B to Lattice's Holoscan sensor bridge FPGA board
- Implemented link layer with frame building and PCS physical layer to convert JESD204B packets to Ethernet at 6.125 Gbps

Academic Extracurriculars

Analog Design Team Lead | Silicon Jackets *May 2026 – Present*

- Leading the first collegiate analog mixed-signal IC design team, defining roadmaps and methodology for 20+ members
- Architecting co-simulation and PnR integration to bring analog blocks to SiliconJackets' SKY130 tape-out flow
- Growing the team's scope to include RF and audio/signal processing projects

Analog Mixed-Signal Design Engineer | Silicon Jackets *October 2025 – May 2026*

- Engineered schematic & layout for ring VCO, buffer, single stage amplifier, and digital inverter using Cadence Virtuoso/Pegasus, simulated using Maestro (ADE Explorer/Assembler)
- Designing an 8-bit R-2R DAC, validating with transient/AC/Monte-Carlo simulation

Digital Design Engineer | Silicon Jackets *January 2025 – Present*

Tape-out 1:

- Achieved tape-out of 6-stage RISC-V core with 4KB of DFFRAM on SkyWater 130nm
- Designed a SystemVerilog module through full stack (RTL, testbench, static timing analysis, P&R) to calculate greatest common denominator using the Euclidean algorithm (99.62% DUT coverage)
- Programmed a Python script to parse STA reports and identify setup/hold violations

Tape-out 2:

- Implemented block diagrams, state machines, Python code, and RTL for a fast divider module on RISC-V core
- Verified via UVM testing environment with constrained random verification (10k+ test points) and directed testing

Tape-out 3:

- Building and verifying a pipelined CORDIC AXI peripheral
- Performing bit-level C simulation to drive architectural design choices

Projects

Low-Power AI Inference SoC *February 2026 – Present*

- Leading a team of 6 building a RISC-V CPU with a multiply-accumulate/DFT accelerator and custom SRAM
- Designing and verifying custom SRAM architecture using half-swing pulse-mode gate family for low power AI inference
- Researching power-reduction techniques including memory partitioning and quiet-bitline architecture